A2 Cancel. signal and the WEB signal refers to a write enable signal. The last character "B" refers to a bar-triggered-enable signal.

IN THE CLAIMS

1. (Amended) A circuit, comprising:

a read charge control circuit activated only during read operations by a read signal and an address; and

a write charge control circuit activated by a write signal and the same or a different address, the read charge control circuit and the write charge control circuit both coupled to common data IO lines.

A3 2. (Amended) The circuit according to claim 1 wherein the read charge control circuit is a sense amplifier.

Sub B1 3. (Amended) The circuit according to claim 1 wherein the write charge control circuit transfers charge between the data IO lines and bit lines.

4. (Amended) The circuit according to claim 1 wherein the write charge control circuit includes only two write controlled gates, a first one of the write controlled gates controlling charge of a bit line and a second one of the write controlled gates controlling charge of a complementary bit line.

5. (Amended) The circuit according to claim 4 wherein the first and second write controlled gates are both controlled by a write column select line signal.

6. (Amended) The circuit according to claim 4 wherein the first write controlled gate is coupled directly between the bit line and a data IO line and the second write controlled gate is coupled directly between the complementary bit line and a complementary data IO line.

7. (Amended) The circuit according to claim 1 wherein the read charge control circuit includes a first read controlled gate controlling charge from a bit line to a

complementary data IO line and a second read controlled gate controlling charge from a complementary bit line to a data IO line.

8. (Amended) The circuit according to claim 7 wherein the first and second read controlled gates are both controlled by a read column select line signal.

9. (Amend) The circuit according to claim 7 wherein the first read controlled gate is coupled directly between the bit line and the complementary data IO line and the second read controlled gate is coupled directly between the complementary bit line and the data IO line.

10. (Amend) The circuit according to claim 1 including a data output sense amplifier coupled between a data output buffer and the data IO lines.

11. (Amended) The circuit according to claim 10 including load transistors shared between the read charge control circuit and the data output sense amplifier.

12. (Amended) The circuit according to claim 1 wherein the read charge control circuit includes:

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to a complementary data IO line and a third terminal;

a second transistor having a first terminal coupled to a complementary bit line, a second terminal coupled to a data IO line and a third terminal; and

a third transistor having a first terminal coupled to a column select line, a second terminal coupled to the third terminal of the first and second transistor and a third terminal coupled to a first reference voltage.

13. (Amended) The circuit according to claim 12 wherein the write charge control circuit includes:

a first transistor having a first terminal coupled to a write column select line, a second terminal coupled to the complementary bit line and a third terminal coupled to the complementary data IO line; and

a second transistor having a first terminal coupled to the write column select line, a second terminal coupled to the data IO line and a third terminal coupled to the bit line.

14. (Amended) The circuit according to claim 13 including a first load transistor having a first terminal coupled to a second reference voltage, a second terminal coupled to the data IO line and a third terminal coupled to a third reference voltage; and a second load transistor having a first terminal coupled to the second reference voltage, a second terminal coupled to the complementary data IO line and a third terminal coupled to the third reference voltage.

15. (Amended) A circuit, comprising:

a read charge control circuit activated by a read column select line;

a write charge control circuit activated by a write column select line, wherein the read charge control circuit and the write charge control circuit are both coupled to common data IO lines;

a data output sense amplifier; and

load transistors shared by both the read charge control circuit and the data output sense amplifier.

Cancel claims 16-33.

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34. (New) The circuit of claim 15, wherein the write charge control circuit is activated independently of the read column select line used for activating the read charge control circuit.

35. (New) The circuit of claim 15, wherein the read charge control circuit is a sense amplifier.

36. (New) The circuit of claim 15, wherein the write charge control circuit transfers charge between the common data IO lines and bit lines.

37. (New) The circuit of claim 15, wherein the write charge control circuit includes only two write controlled gates, a first one of the write controlled gates controlling charge of a bit line and a second one of the write controlled gates controlling charge of a complementary bit line.

38. (New) The circuit of claim 37, wherein the first and second write controlled gates are both controlled by a write column select line signal.

39. (New) The circuit of claim 37, wherein the first write controlled gate is coupled directly between the bit line and data IO line and the second write controlled gate is coupled directly between the complementary bit line and a complementary data IO line.

40. (New) The circuit of claim 15, wherein the read charge control circuit includes a first read controlled gate controlling charge from a bit line to a complementary data IO line and a second read controlled gate controlling charge from a complementary bit line to a data IO line.

41. (New) The circuit of claim 40, wherein the first and second read controlled gates are both controlled by the read column select line.

42. (New) The circuit of claim 40, wherein the first read controlled gated is coupled directly between the bit line and the complementary data IO line and the second read controlled gate is coupled directly between the complementary bit line and the data IO line.

43. (New) The circuit of claim 15, wherein the data output sense amplifier is coupled between a data output buffer and the common data IO lines.

44. (New) The circuit of claim 15, wherein the read charge control circuit includes:

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to a complementary data IO line and a third terminal;

a second transistor having a first terminal coupled to a complementary bit line, a second terminal coupled to a data IO line and a third terminal; and

a third transistor having a first terminal coupled to the read column select line, a second terminal coupled to the third terminal of the first and second transistors and a third terminal coupled to a first reference voltage.

45. (New) The circuit of claim 44, wherein the write charge control circuit includes:

a first transistor having a first terminal coupled to the write column select line, a second terminal coupled to the complementary bit line and a third terminal coupled to the complementary data IO line; and

a second transistor having a first terminal coupled to the write column select line, a second terminal coupled to the data IO line and a third terminal coupled to the bit line.

46. (New) The circuit according to claim 45 including

a first load transistor having a first terminal coupled to a second reference voltage, a second terminal coupled to the data IO line and a third terminal coupled to a third reference voltage; and

a second load transistor having a first terminal coupled to the second reference voltage, a second terminal coupled to the complementary data IO line and a third terminal coupled to the third reference voltage.